1. The switchboxes may contain more wires in the vertical direction than in the horizontal direction because the channels in an FPGA are usually arranged vertically to compensate for the number of wires from the LUTs.
2. The size of the bitstream is:

IO:

LUTs:

Wires: FPGA is 500x500 LUTs (

Switchboxes:

Wires to LUTs =

Total Bits for full FPGA:

Since we use 65% of the LUTs and 79% of the switchboxes:

Bitstream size:

1. The percentage of unspecified bits in the bitstream is:

Therefore, 23.55% of the bits are unspecified.

1. Distinct bitstreams:
   1. 13 possible configurations for the 50 IO pads = possible configurations
   2. 65% of 250,000 = 162,500 LUTs being used. Each of which can be programmed different ways. possible configurations
   3. 79% of the switchboxes.

Each switchbox can be configured different ways =

* 1. Total number of distinct bitstreams:

different ways